

line 5, delete "issues in".

line 8, delete "design" and insert --circuit--;

line 8, delete "part" and substitute --DUT--.

line 9, delete "device" and substitute --DUT--.

line 11, delete "system" and substitute --circuit--;

line 11, delete "datacom".

IN THE CLAIMS

Please amend Claims 1-7 as follows:

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1. (Amended) Apparatus for testing an integrated circuit, comprising:
a data [Data] source [for inputting] coupled to provide test signals to [into] an integrated circuit being tested;
a [A] plurality of relays selectively connecting the integrated circuit being tested to the apparatus;
a plurality of fan [Fan] out elements [receiving] coupled to receive data pulses from the [integrated circuit being tested] relays and [connected] to distribute the data pulses to a plurality of latches; and
a [A] strobe element associated with each latch thereby enabling each latch to transfer the data pulses from an input port [its input ports] to an output port of each latch [its output ports].

2. (Amended) The apparatus of claim 1, [wherein] further comprising testing components each coupled to receive the [unique] data pulses from one of the plurality of latches [at a fixed time interval from the time at which each latch is enabled to transfer data pulses from its input ports to its output ports], the [said] testing components receiving the data

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pulses at a frequency that is a fraction of the output signal frequency of the integrated circuit being tested.

3. (Amended) The circuit network of claim 2, wherein the fraction is equal to the output frequency of the integrated circuit being tested divided by the number of the latches [in the apparatus].

4. (Amended) A method [of testing an integrated circuit], comprising the acts of:
providing an integrated circuit;

applying signals to the integrated circuit;

fanning out data pulses received from an output port of the [an] integrated circuit [being] tested;

distributing the data pulses each to one of [to] a plurality of latches; and

calibrating a time at which each one of the plurality of latches is enabled. [;]

5. (Amended) The method of claim 4, further comprising the acts of [wherein a clock signal of the integrated circuit being tested and a clock signal of a tester are synchronized by the method comprising]:

measuring the time between initialization of the integrated circuit [being tested] and detection of a first data pulse at an input port of a selected one of the

plurality of latches [latch];

calculating a [the] clock frequency of the integrated circuit [tested device] therefrom, and;

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